Designing and Verifying Future High Speed Busses

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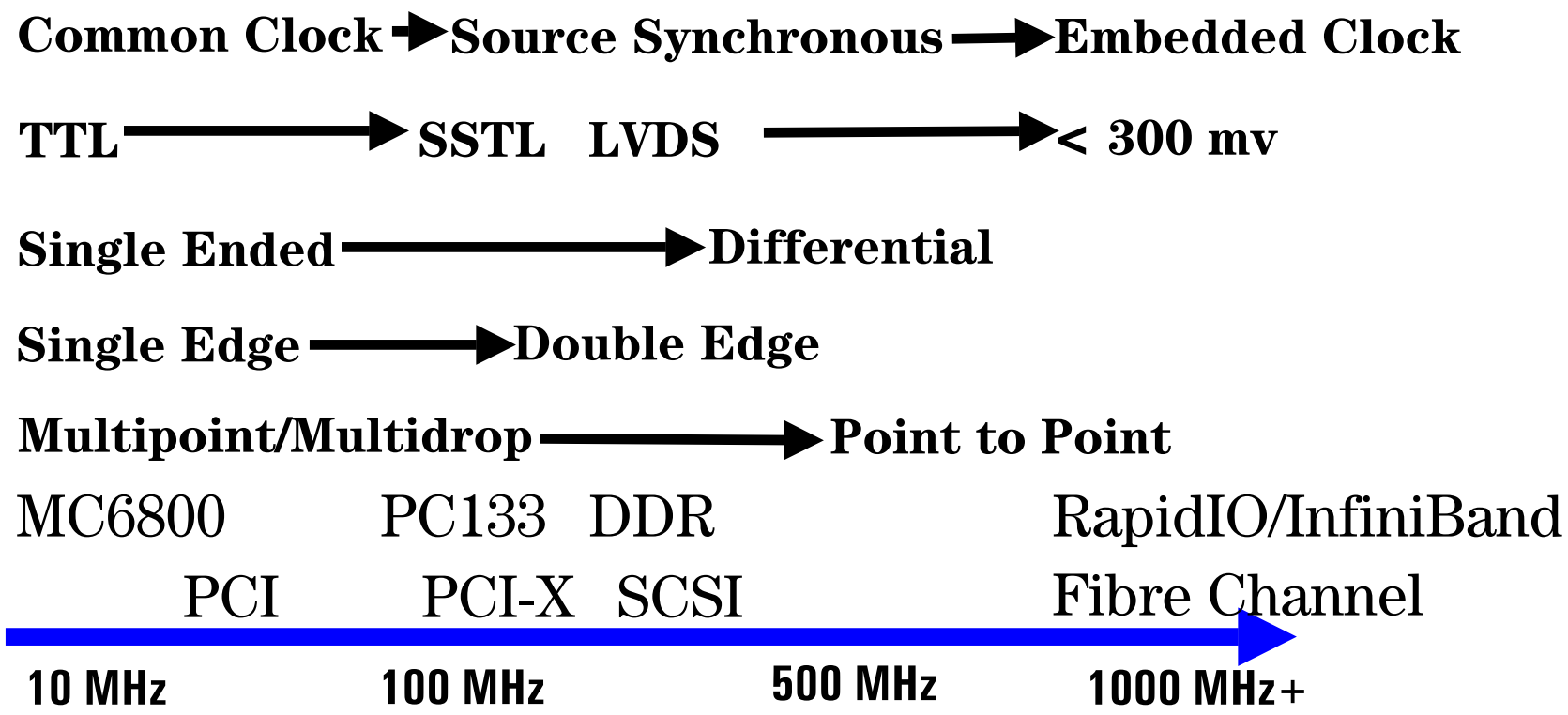
Power Tools For Bus Analysis

Agilent Technologies
Innovating the HP Way

Agenda

- Bus Technology Trends and Challenges
- Making the transition: Design and Test of DDR Busses
- Agilent Technologies and FuturePlus Systems DDR Analysis Solution
- Q&A

Bus Technology Trends



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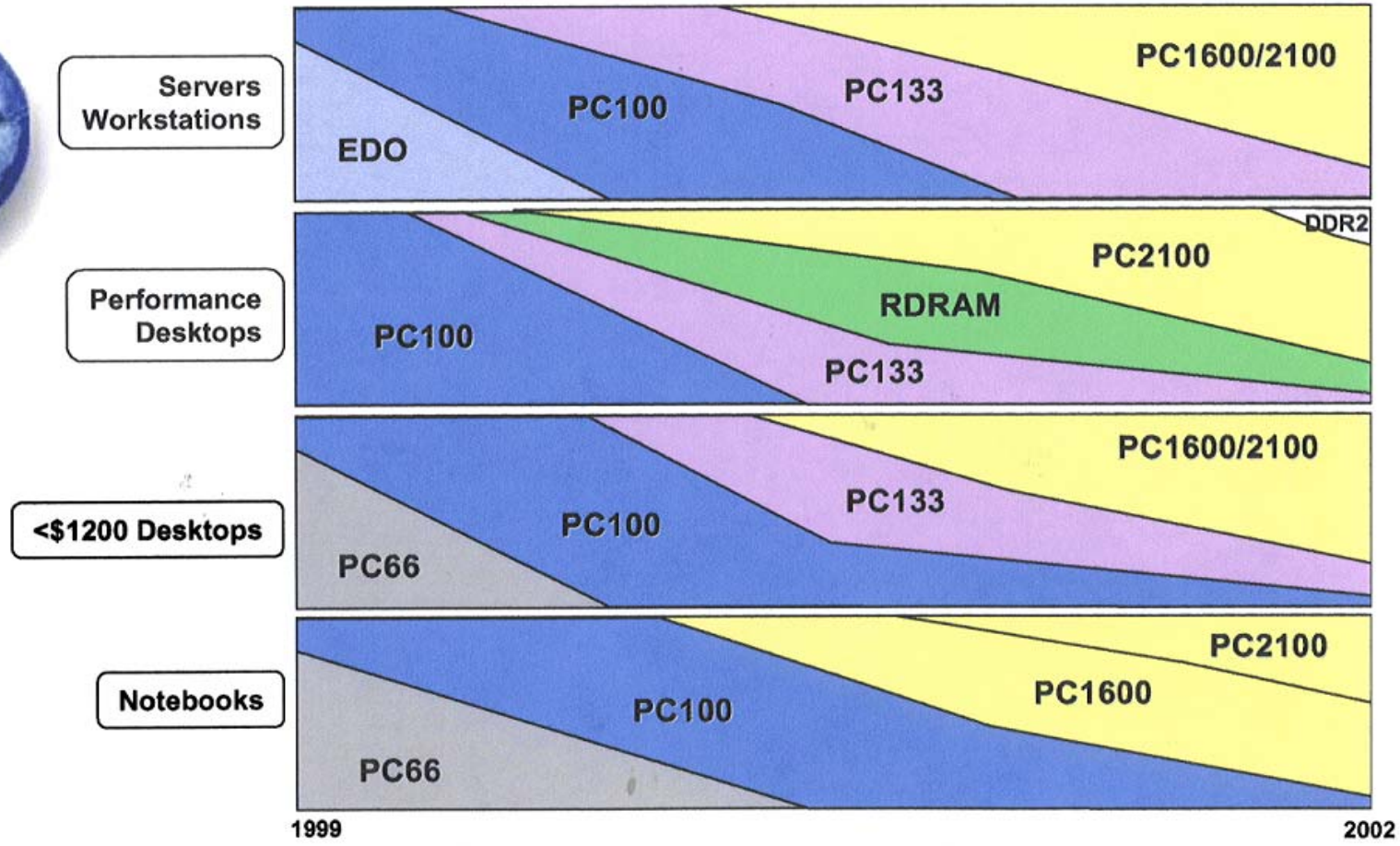
Main Memory Demand Forecast



Advanced Memory International, Inc.

Comparing PC133 and PC266 DDR

	PC133	DDR
Speed	133 Mhz	266Mhz+
Clock Edges	Single	Double
Clock Method	Common	Source Synchronous
#Clocks	1	Up to 19
Eye Size	2V x 4ns	700mv x 1.0ns
Timing	Centered	Centered / Straddle
Interconnect	Multipoint	Multipoint

DDR Technology Challenge: Finding and Maintaining the Data Eye

- Managing jitter budget
  - Crosstalk
  - Intersymbol Interference
  - Clock **AND** Data Jitter
- Managing signal integrity
  - Termination
  - Stubs
  - Signal Loss (Dielectric, Loading)

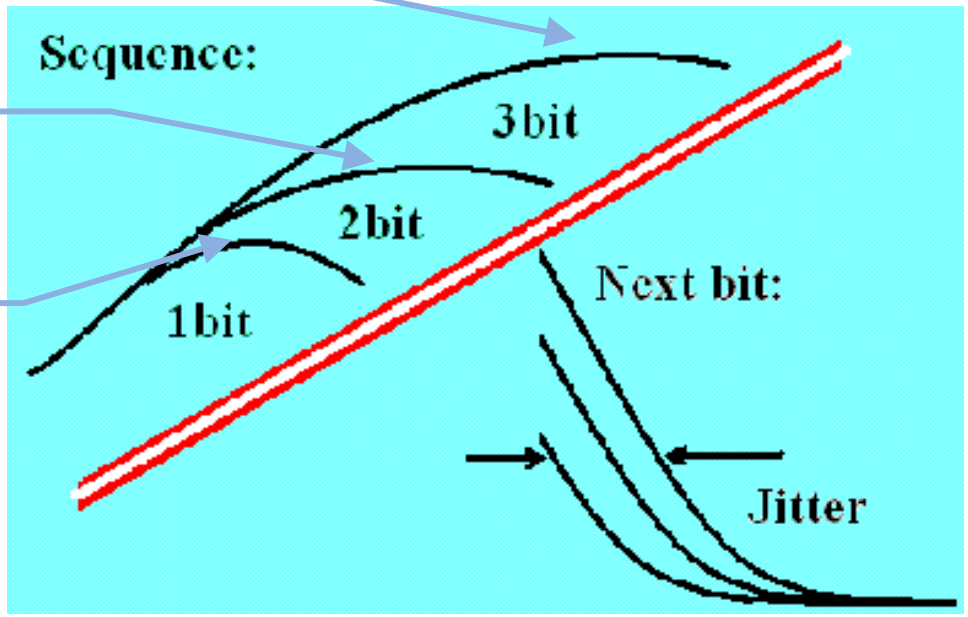
Sources of Jitter on DDR Bus:
Intersymbol Interference

Bit pattern

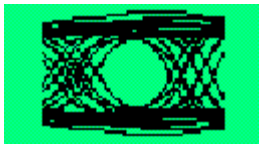
"01110"

"0110"

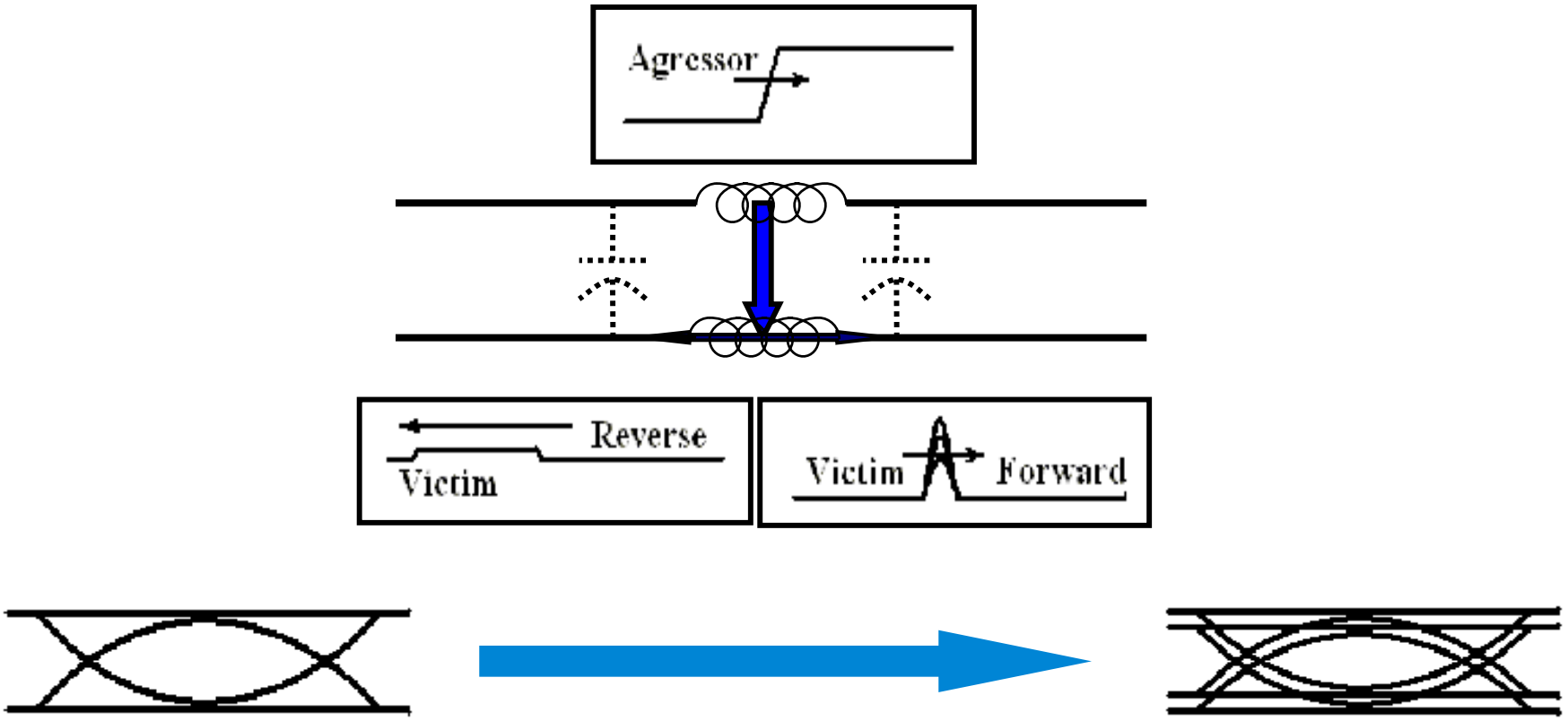
"010"



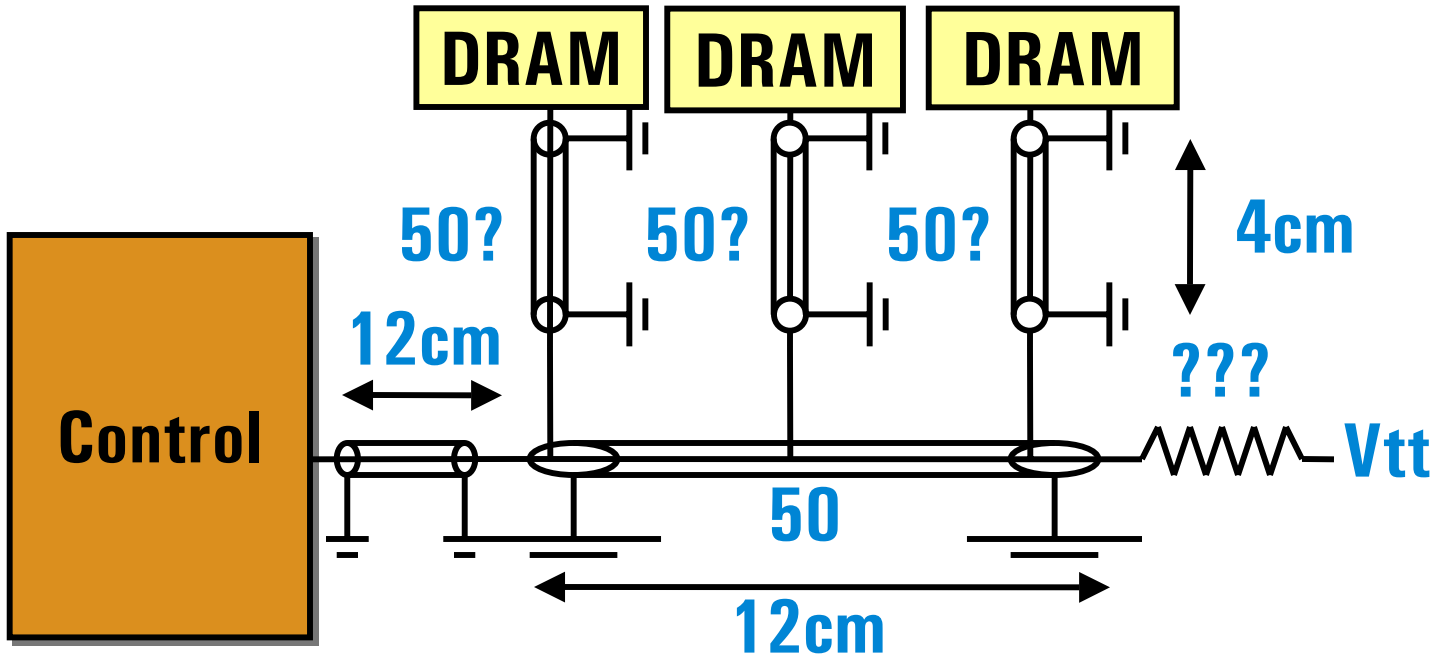
Eye Diagram



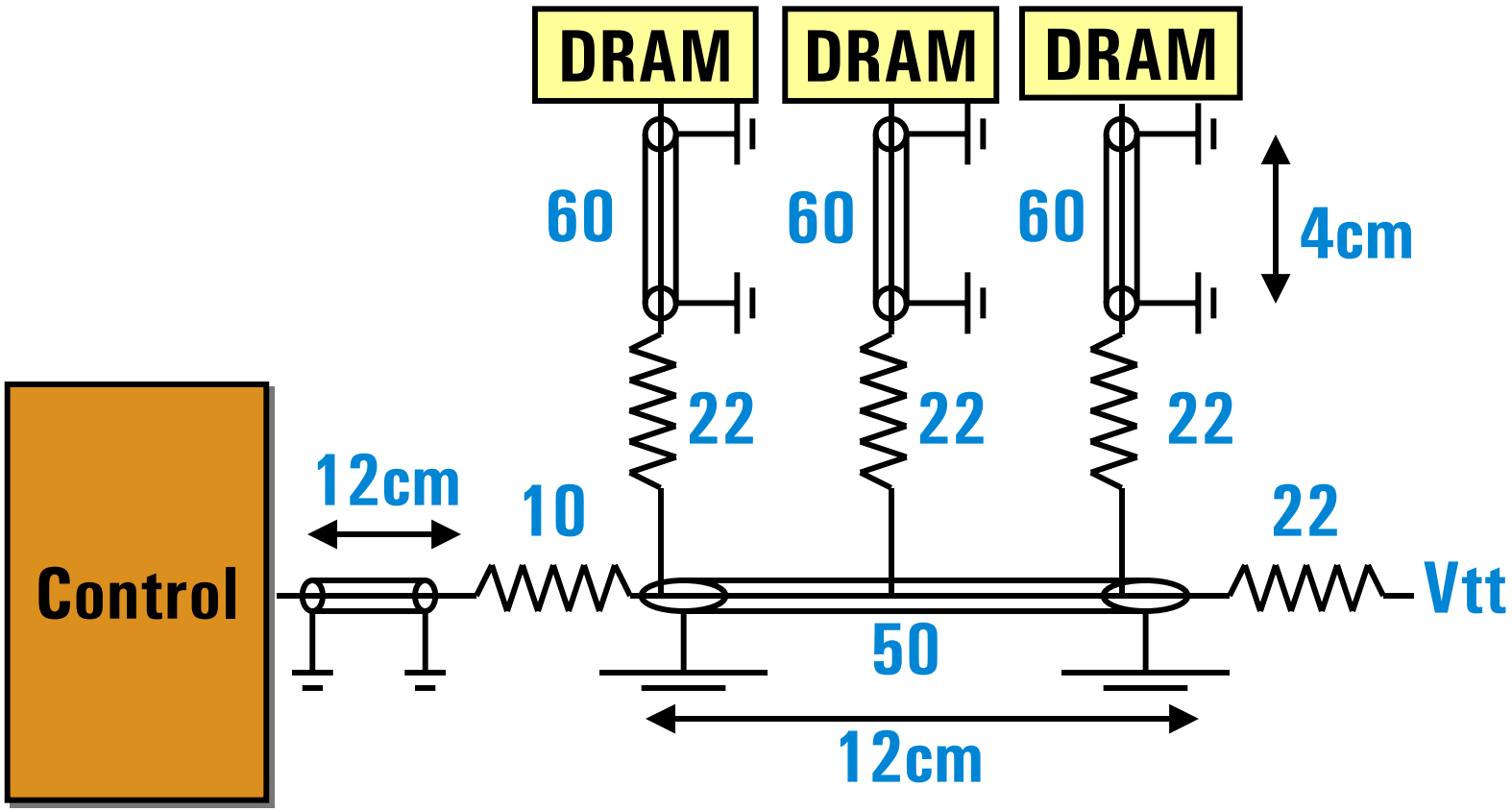
Sources of Jitter on DDR Bus: Crosstalk



DDR Bus Signal Integrity:
Dealing with Stubs



DDR Bus – Where to Terminate?
Answer: Everywhere! (and Nowhere)



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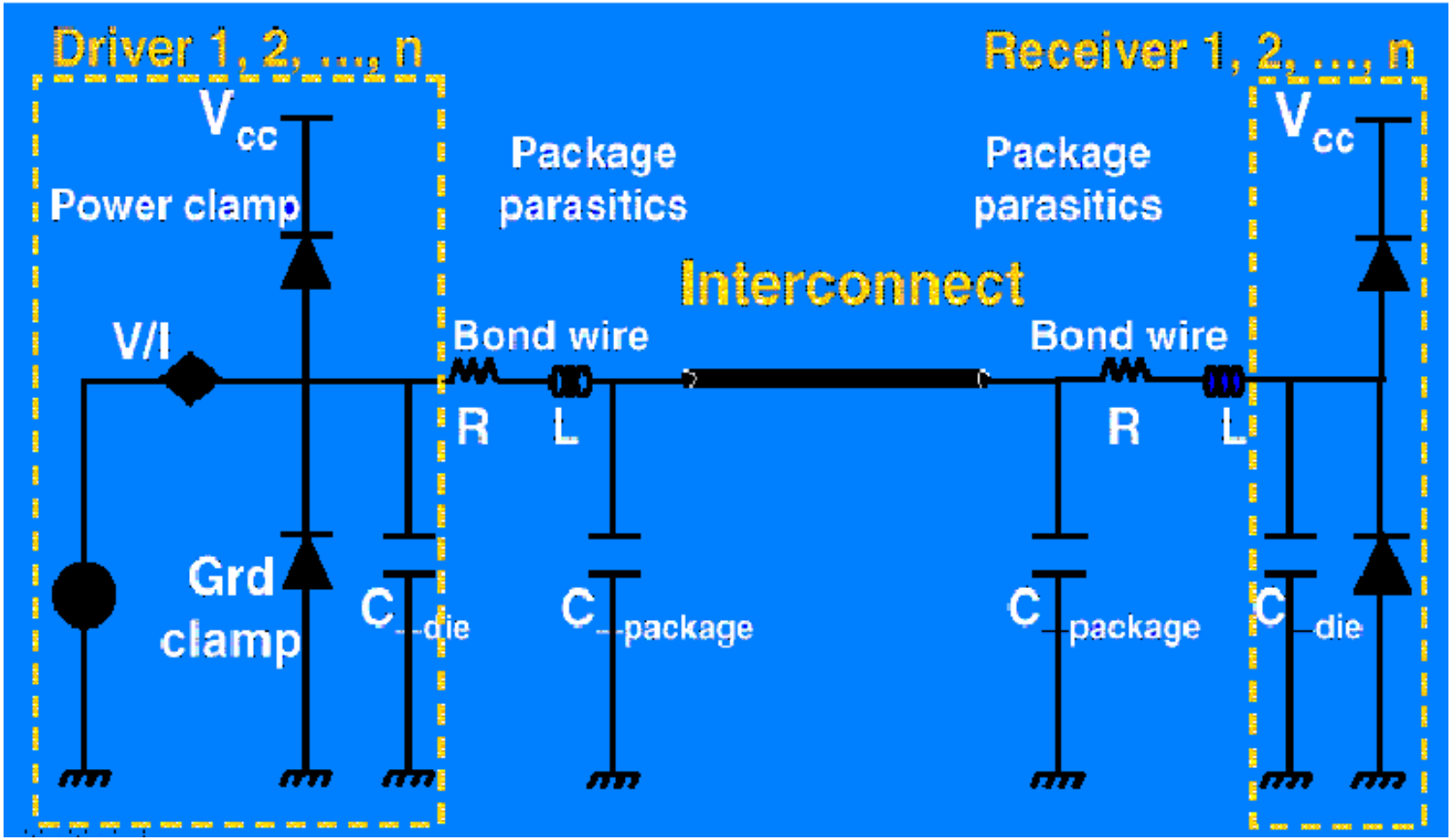
Managing Signal Integrity:

Spice Simulation



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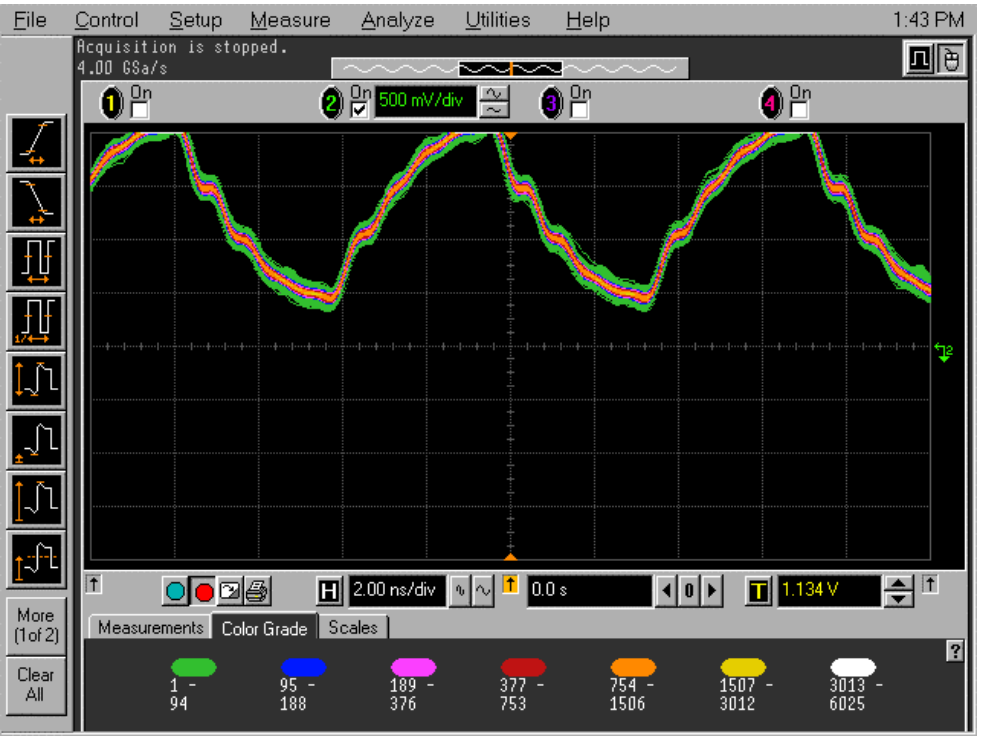
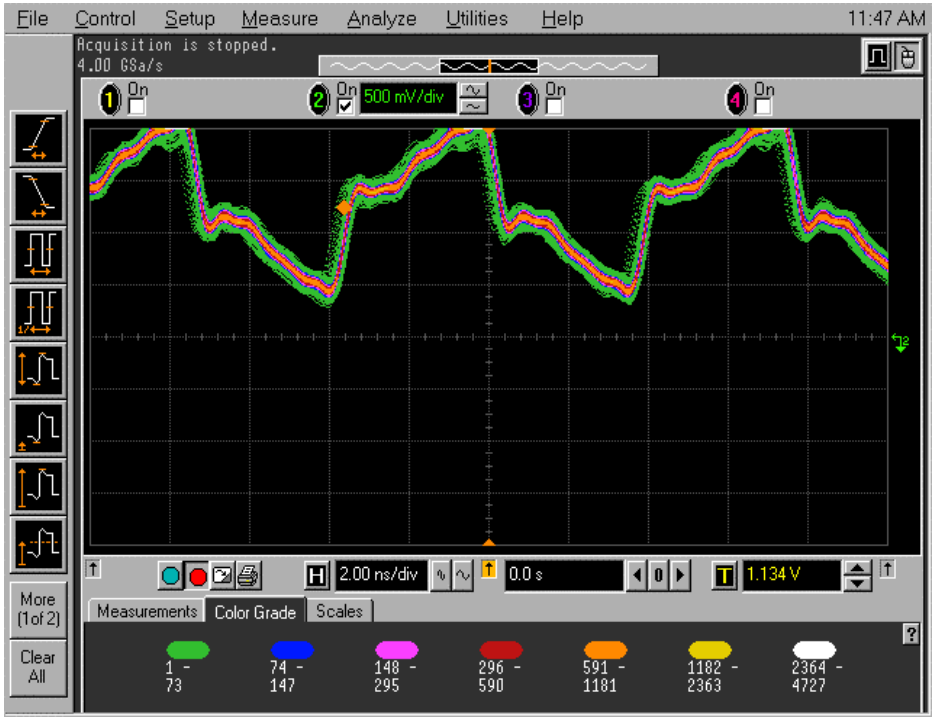
Optimizing Signal Integrity

Almost Optimal



Not Optimal



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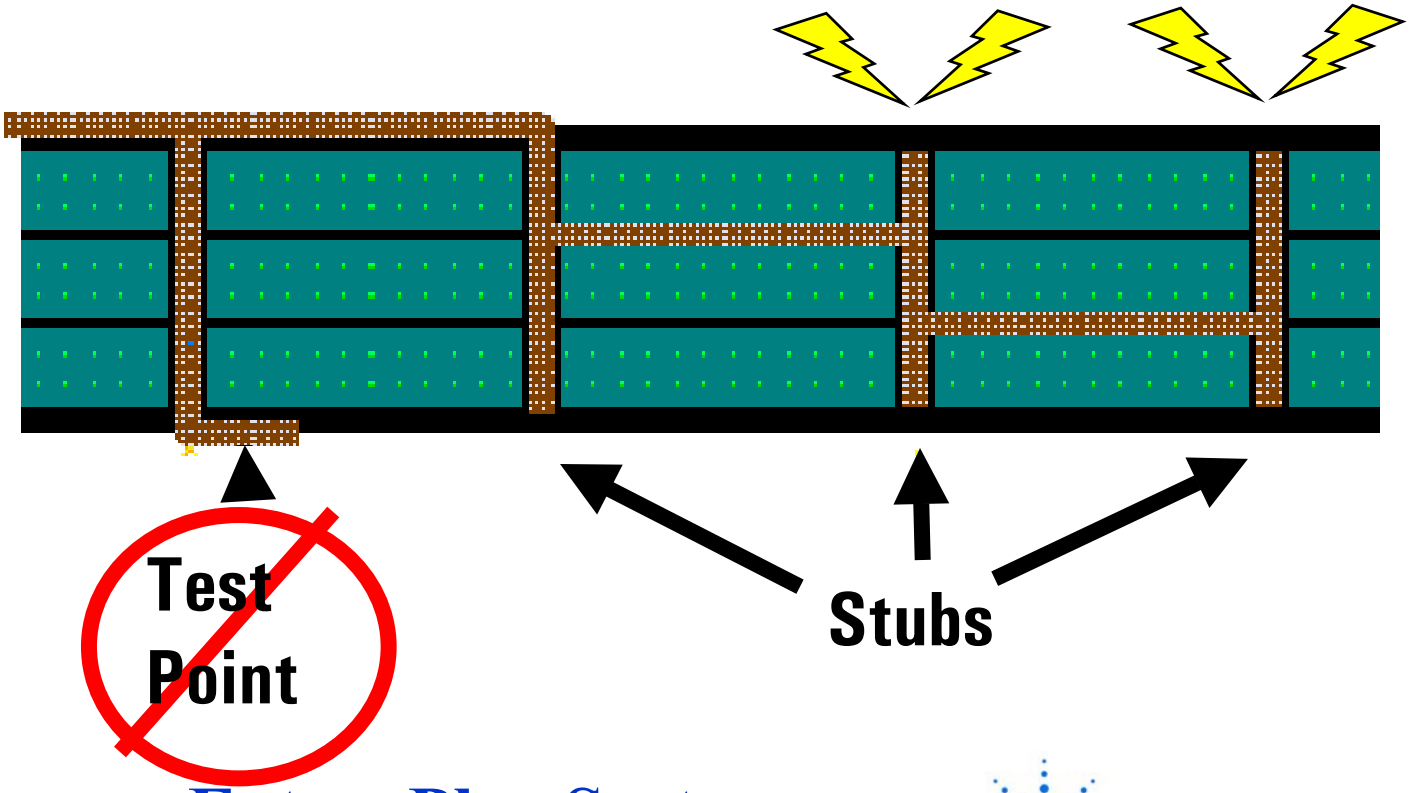
It's Only Going To Get Worse!

Above 1000Mhz vias can become stubs!



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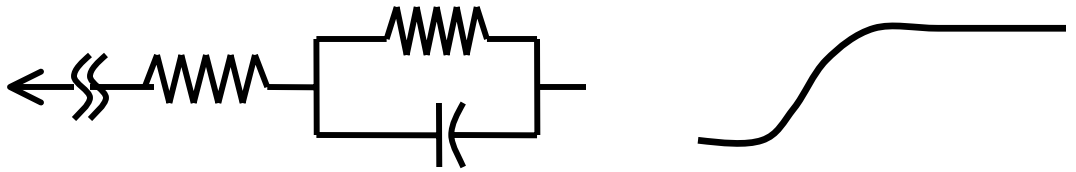
DDR Validation – Tools You Will Need

- Required Tools:
  - High Frequency Oscilloscope (1.5Ghz)
  - Logic State and Timing Analyzer with DDR Bus Probe
  - Spice Simulator
- Useful Tools
  - Time Domain Reflectometry (TDR)
  - Network Analyzer

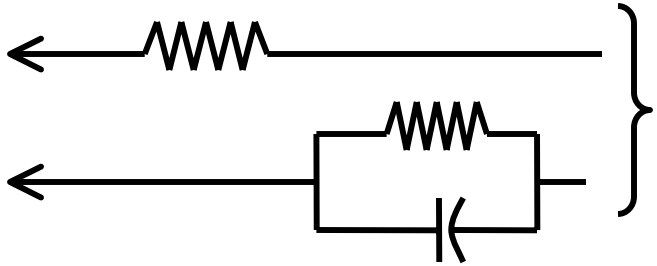
Probing at DDR Frequencies

Input Circuit

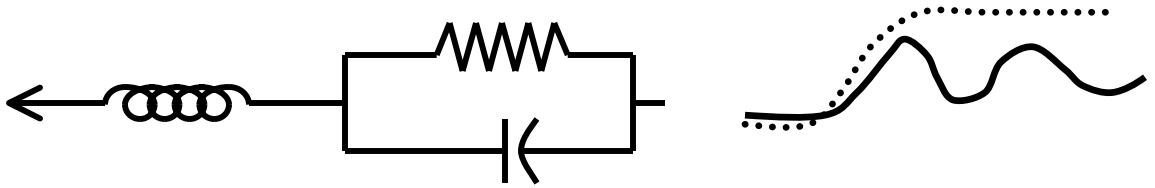


@ 10-20 MHz

@ 20-50 MHz

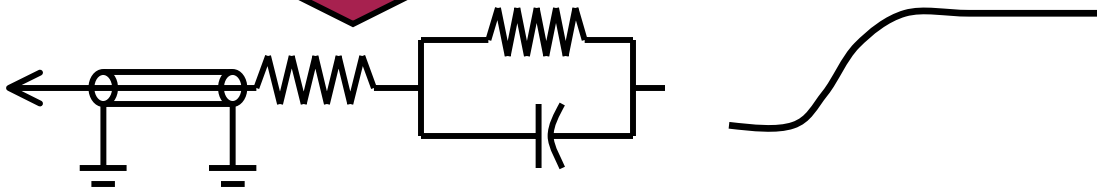


@ > 50 MHz



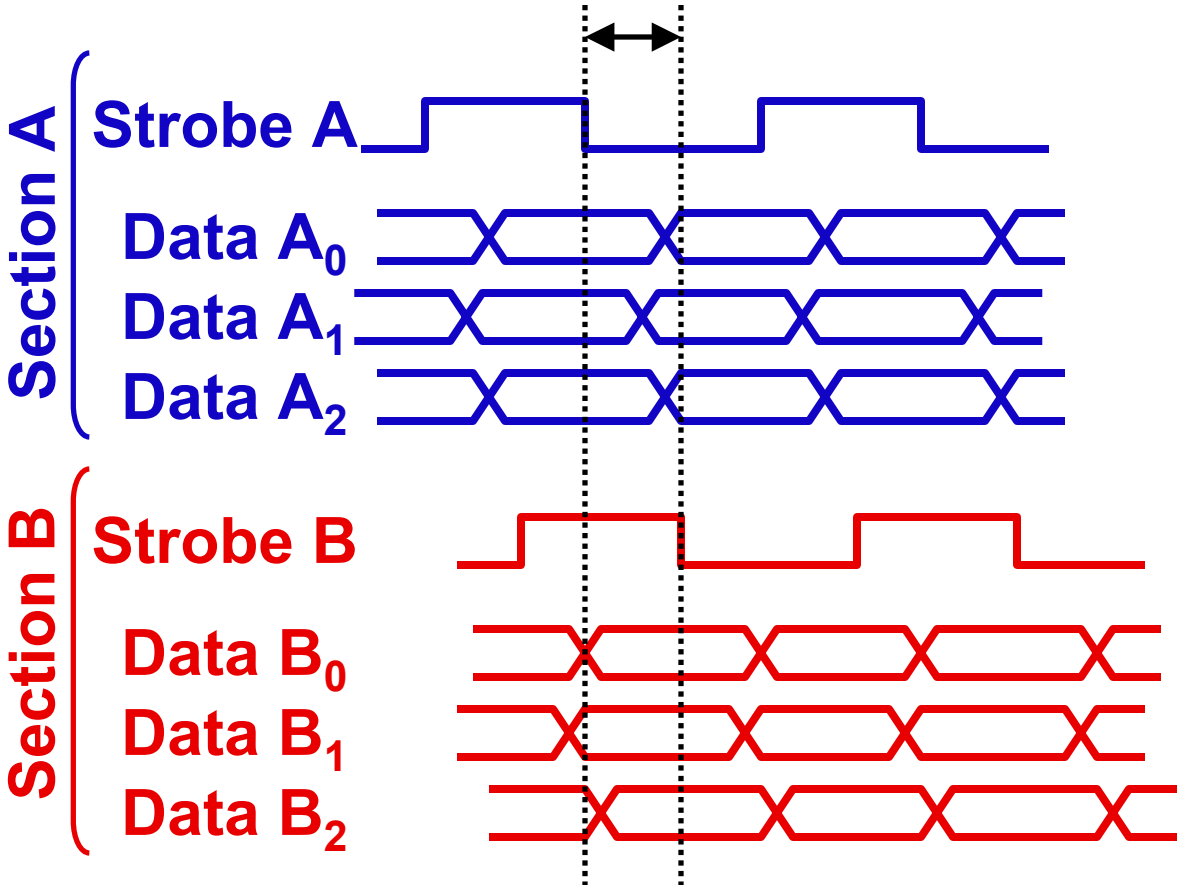
Solution

@ 266+ MHz



Logic Analyzer Sampling - Which Clock to Use?

- Logic Analyzers cannot sample using 19 clocks - only one can be chosen
- Skews between Sections may be large
- Traditional solution requires an active probe



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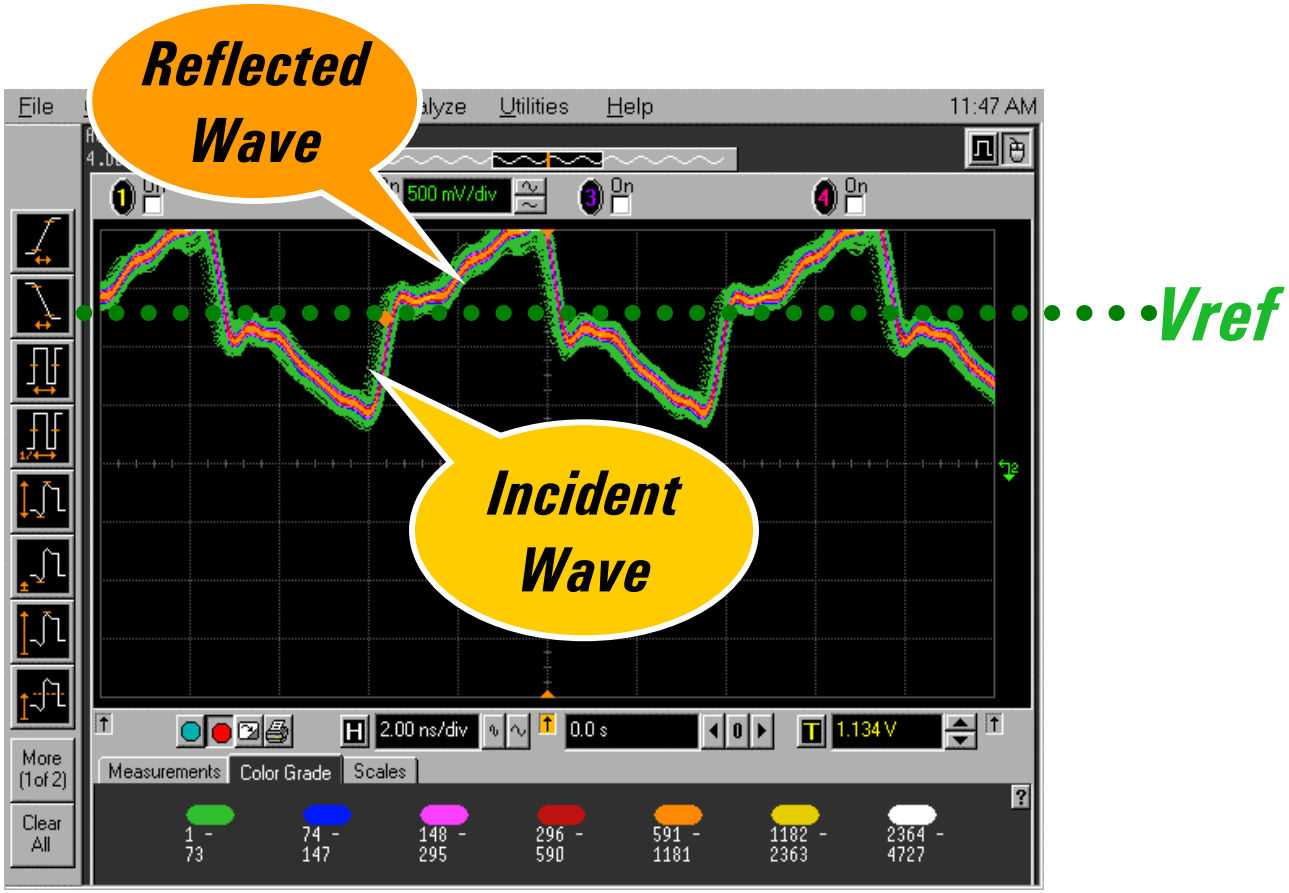
DDR Clock Generation:
Where is the real clock edge?



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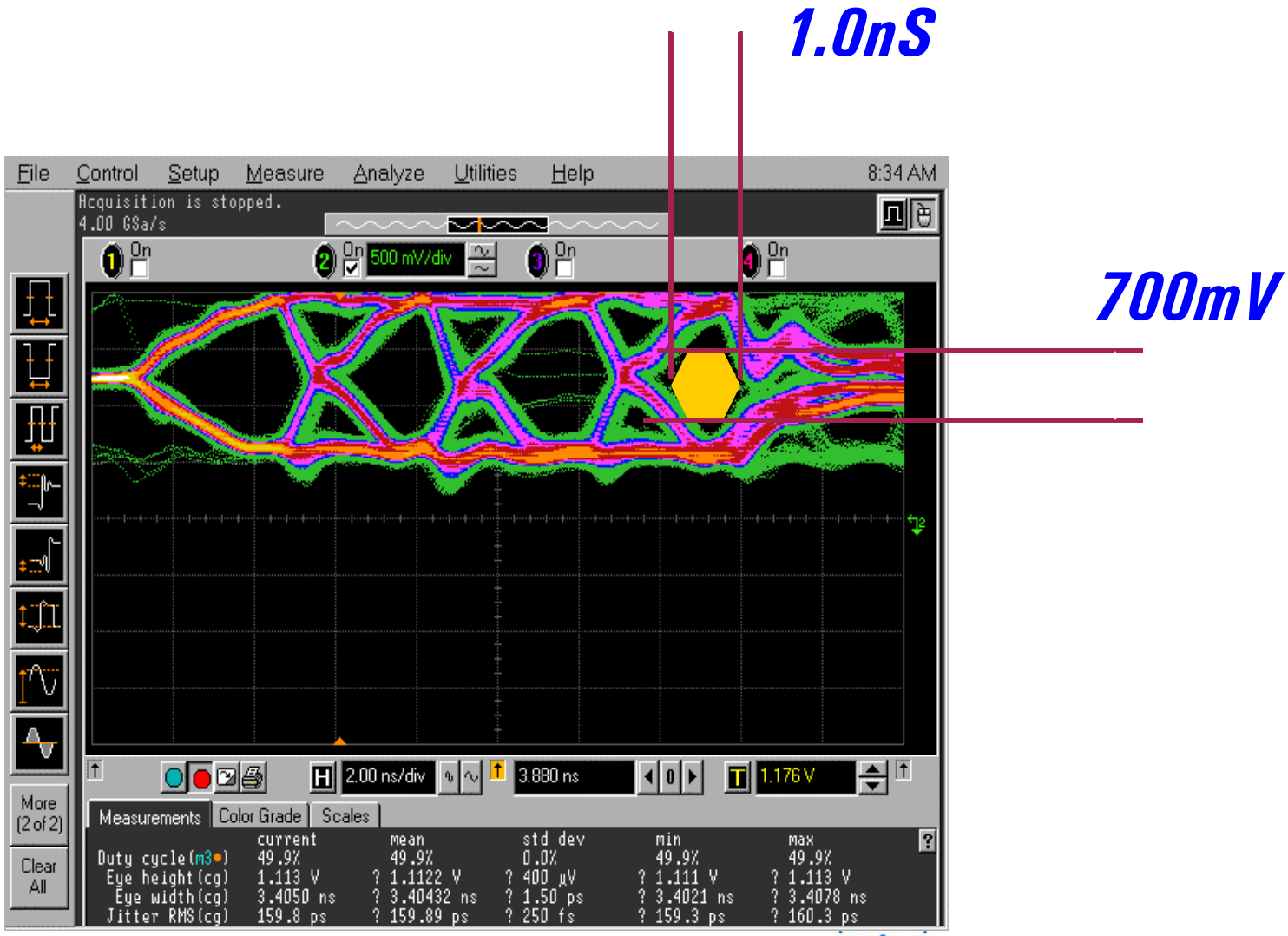
DDR Data Sample Window



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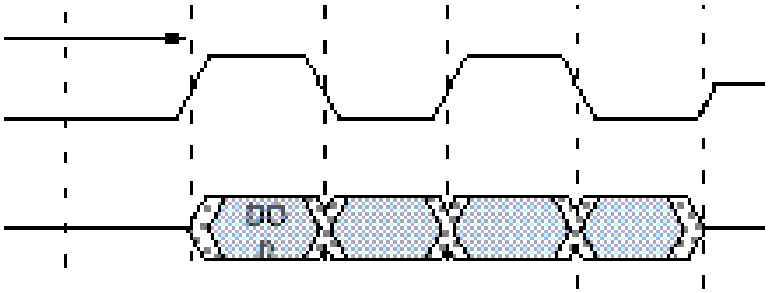
DDR Burst Timing - Read or Write?

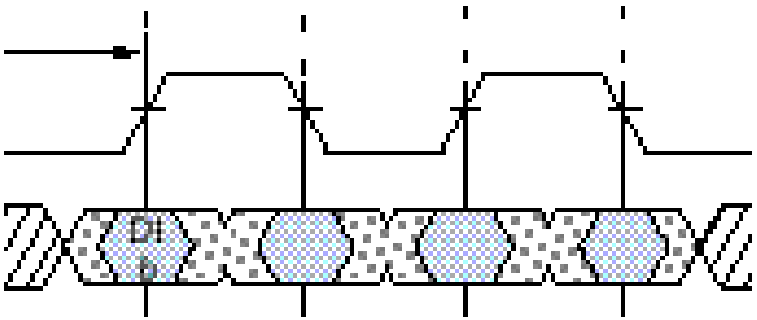
- Clock straddles data

Read



- Clock centered on data

Write



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Ideal DDR Analysis Probe

Active Benefits
+Easy Triggering
+Easy Set-up
+Higher Speeds
+Smaller Aperture

Passive Benefits
+Parametric Measurements
+Low Cost
+Early Availability
+Size and +Heat Load

Passive Probe with State Clock Generation

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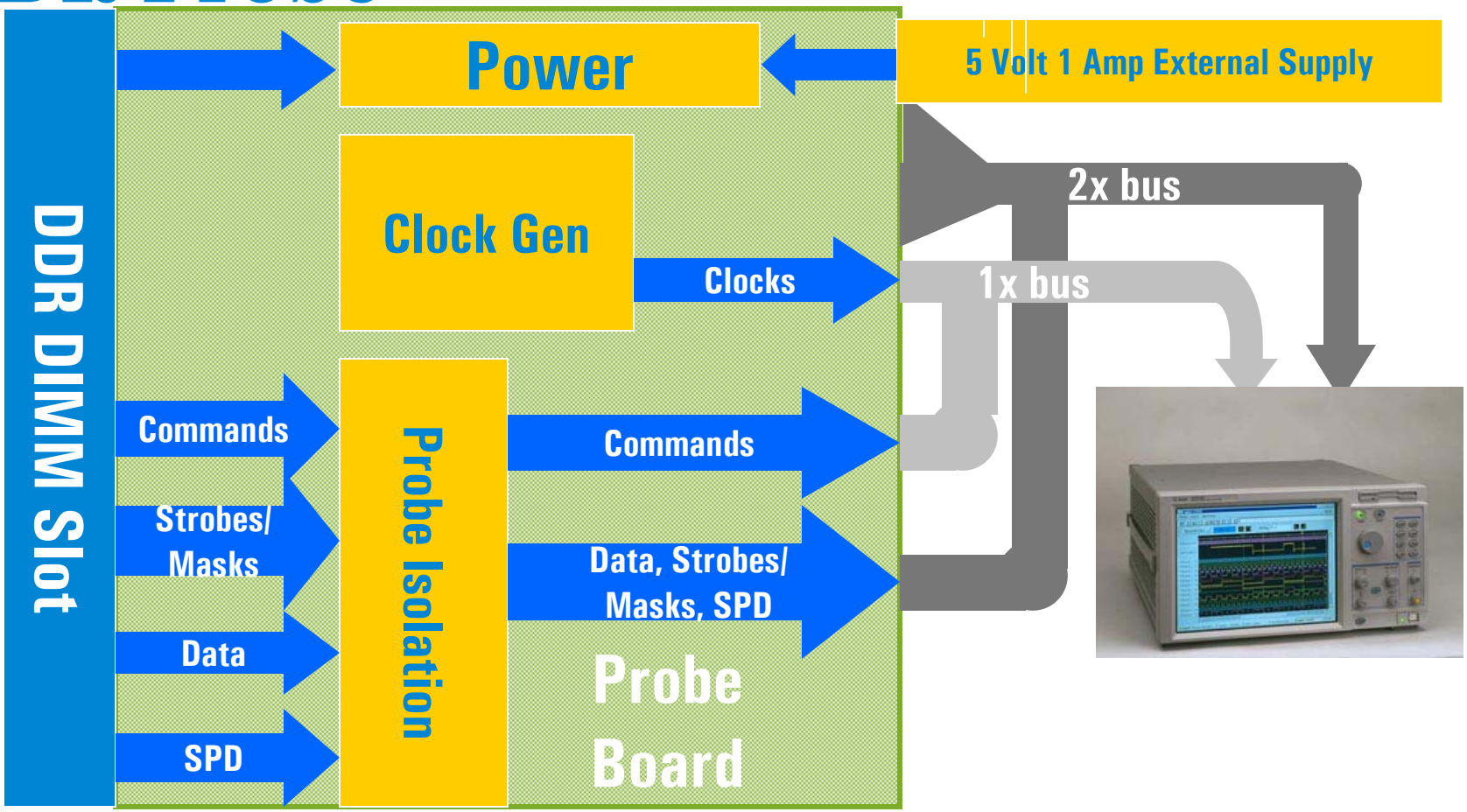
FS2330 (Agilent FSI-60049) Passive DDR Probe



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FS2330 (FSI-60049) DDR DIMM Logic Analyzer Probe

- State and Timing Analysis to PC2662 GHz Timing Analysis concurrent with State Analysis
- Standard DIMM size (1.7” x 5.25”)
- Electrically nonintrusive (same as a 1 bank Registered DIMM)
- Measures signals as the DDR memory chips would see them.

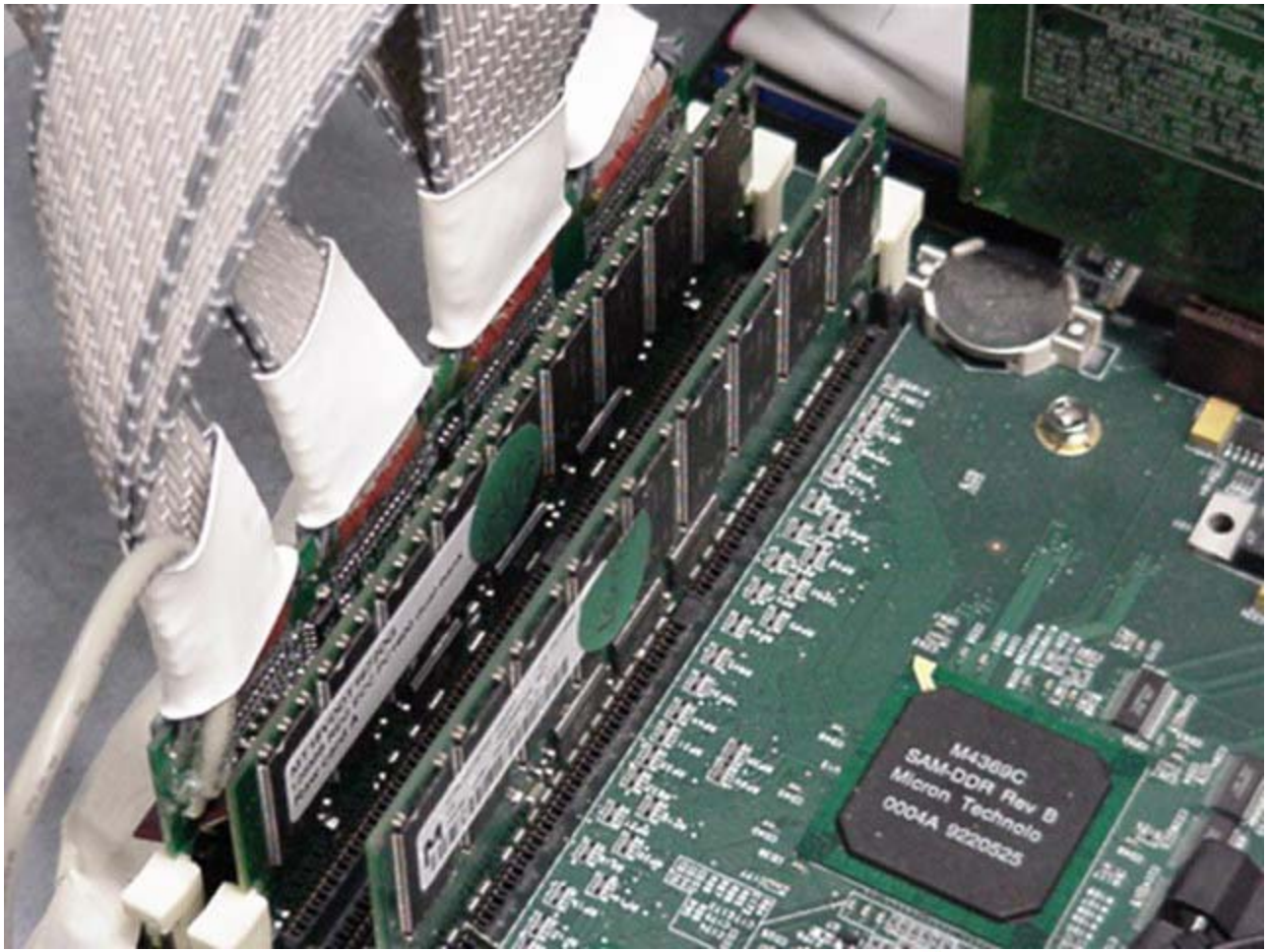
FS2330 Specifications

- All signals are probed passively
- Registered and Non-Registered Dimms supported
  - x4 and x8 SDRAMS
- 64 & 72 bit, 2.5V DIMM supported
- Burst size can be set to 2, 4, 8 or automatic
- Select read only/write only acquisition
- External power supply is required and supplied
- Full inverse assembly
- Protocol sensitive clocking

FS2330 Logic Analyzer Requirements

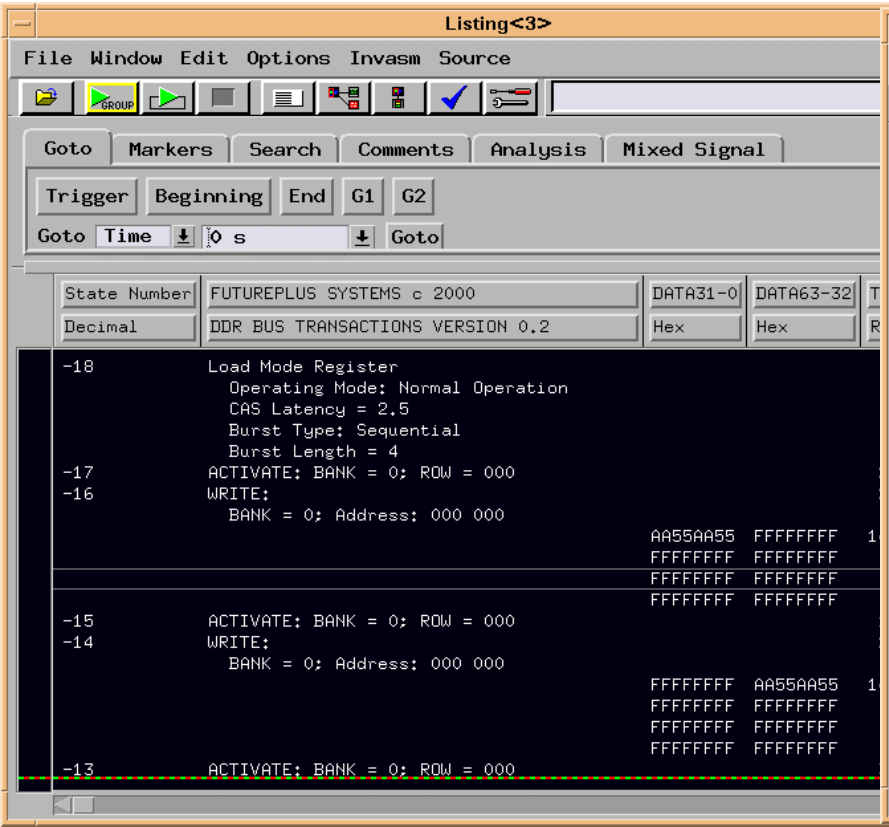
- 1675x support
  - 2 card (PC200), 3 card (PC266) configuration
  - 3 card configuration gives time tags and additional memory depth (8 pods)
- 16715/6/7 Support (PC200, PC266)
  - Turbo Mode required - 3 card solution minimum
- Eye Finder Technology
  - provides characterization
  - automatic alignment of clock and data
  - 100 psec steps

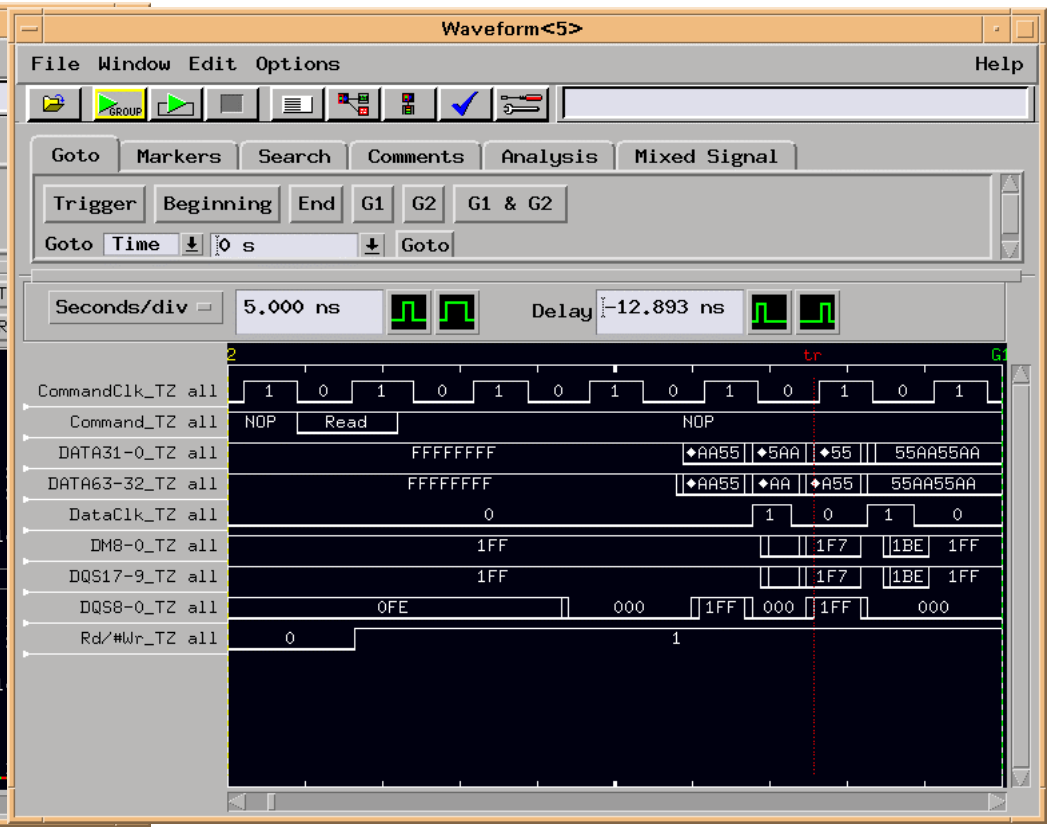
FS2330 DDR Probe Fits In Standard DIMM Slot



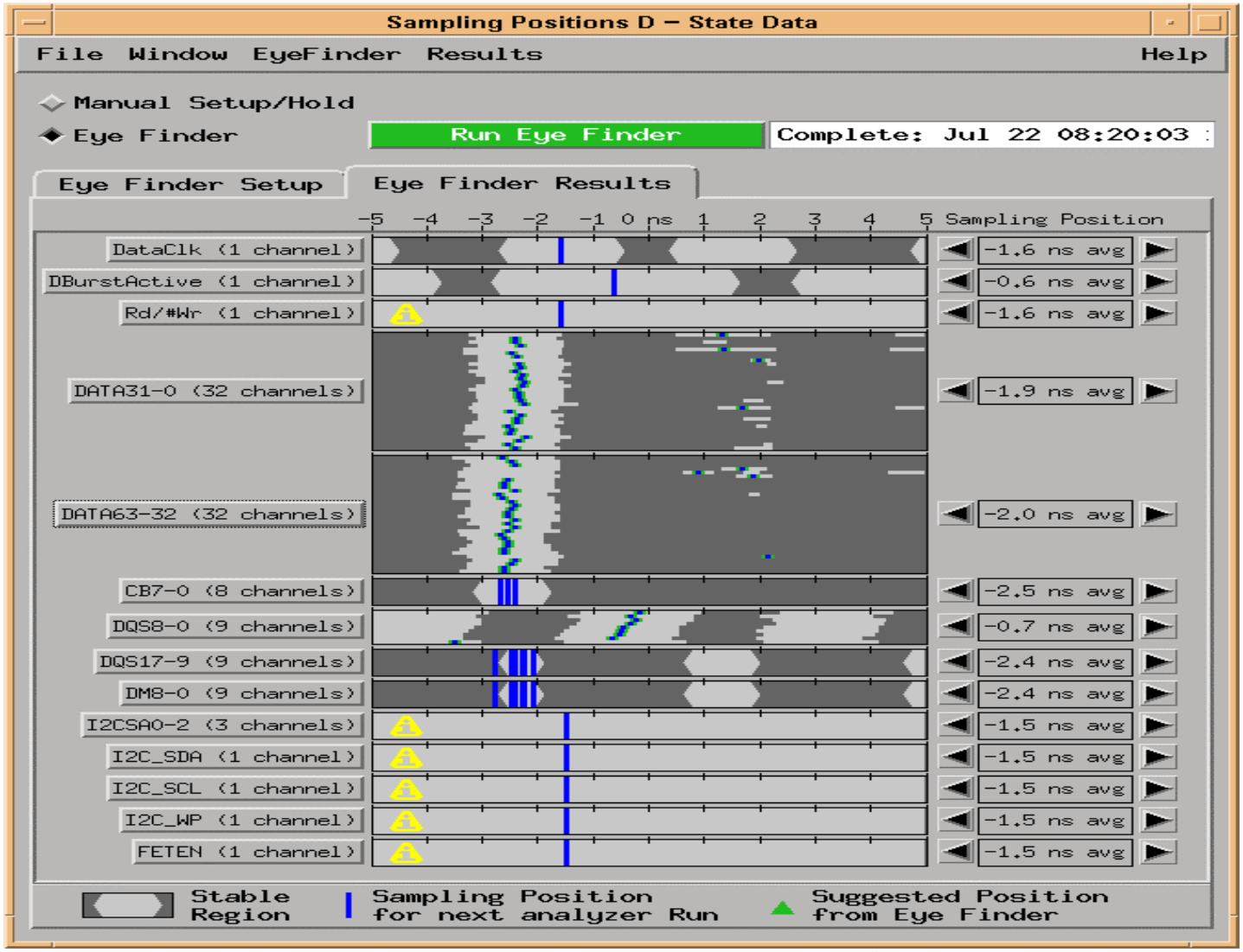
Simultaneous State and Timing Measurements

- Write Data
- Read Bursts





Eye Finder Aligns Clock and Data



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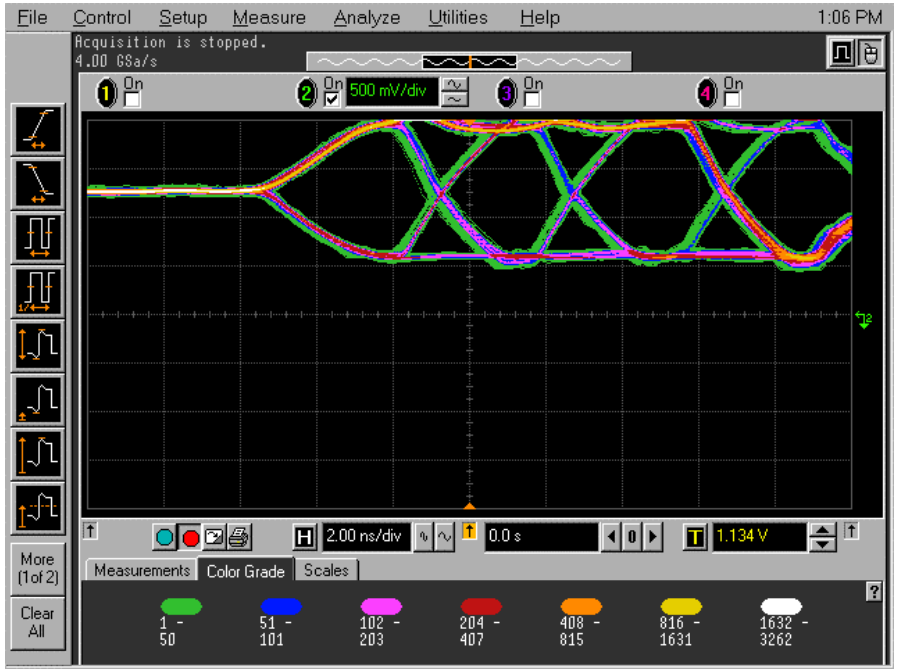
Eye Finder

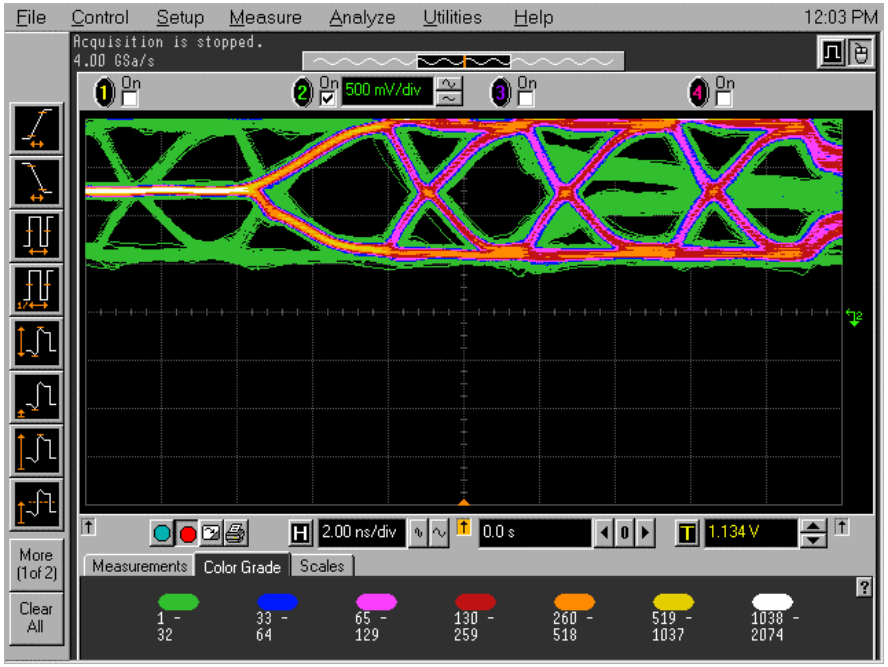
- Aligns data and clock in 100 psec increments
- Automatically aligns data and clock
- Shows size of data eye
- Displays signal skews
- Provides timing/phase relationship of bus signals
- Visually shows possible signal integrity problems
- **All of the above are QUALITATIVE, not QUANTITATIVE**

Reminder
In DDR, Signal Integrity is Important - Especially for Reads

DQ51 Read Near Controller



At Far End of Bus



(also write at end of bus)

B3wrss0192

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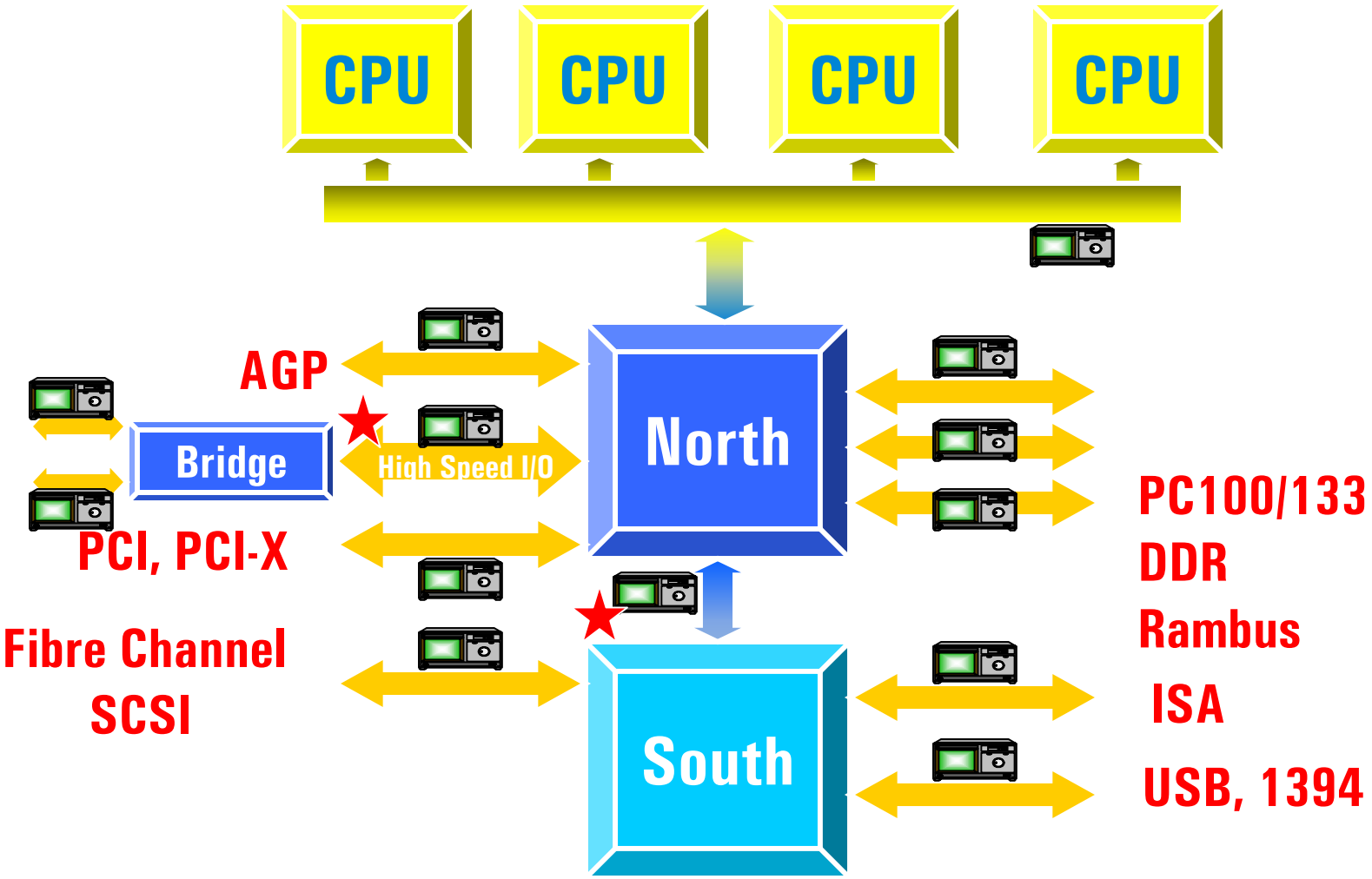
Summary

- The high frequency content of DDR demands attention to design issues
  - Crosstalk, Intersymbol Interference
- The DDR bus should be treated as transmission lines
  - 3D spice modeling
  - Terminations, stubs and antennas

Key Points

- DDR presents new challenges for test tools
  - Source Synchronous clocking
  - Read/Write timing differences
  - Clock detection
- Design debug, verification and validation tools must be transparent to bus
- high speed probing

System Verification



= FuturePlus Systems Solutions

= Agilent Technologies Logic Analyzers

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